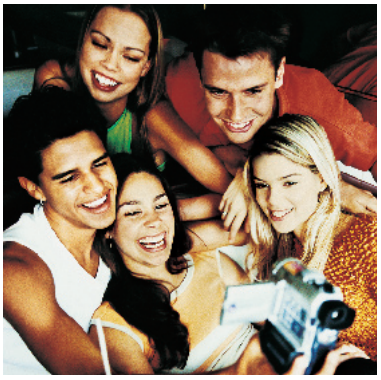
CONNECTIVITY

Data sheet: CN-105



Product code	:	CN-105
Product name	:	USB to VGA Adapter
EAN code	:	8716502005284
Qty. masterpack / carton	:	5/20

Product weight	:	91 gr.
Product dimensions	:	52 (W) x 104 (D) x 24 mm (H)
Gift box weight	:	345 gr.
Gift box dimensions	:	210 (W) x 148 (D) x 45 mm (H)
Masterpack weight	:	2 Kg.
Masterpack dimensions	:	22 (W) x 15,1 (D) x 25,5 cm (H)
Carton weight	:	8,8 Kg.
Carton dimensions	:	46,5 (W) x 33,2 (D) x 28,3 cm (H)

This USB 2.0 to VGA adapter enables you to very easily connect an extra monitor to any computer with a USB port. That could be an extra monitor for your desktop PC, but even if you are using a notebook the USB 2.0 to VGA adapter enables you to enjoy the convenience of an extra monitor via USB at any location.

Box content:

- USB to VGA Adapter
- User manual
- Installation software

System requirements:

- Free USB Port
- Windows 2000, XP

Key features:

- Supports USB 2.0 Standard with a data rate upt o 480 Mbps
- Supports suspend and wake-up modes
- Plug & Play compatible

CONNECTIVITY

Data sheet: CN-105

Technical specifications:

- Compliant with EHCI specification.
- Supports SVGA (DB-15) connecter.
- Supported Resolution
  - 1024x768 16bits
  - 800x600 32bits
  - 640x480 32bits

CHIPSET FEATURES (SiS 315E)

- Built-in a high performance 256-bit 3D engine
- Built-in 32-bit floating point format VLIW geometry transform/lighting engine
- Up to 143 MHz 3D engine clock speed

- Peak polygon rate: 10M polygon/sec @ 1 pixel/polygon with Gouraud shaded, point-sampled, linear and bilinear texture mapping

- Peak fill rate: 286 M pixel/sec, 572 M texture/sec @ 10,000 pixel/polygon with Gouraud shaded and two bilinear textured, Z buffered and alpha blended

- Built-in a high quality 3D engine, high performance VLIW T&L engine and an high performance command-balanced T/L queue

- High Performance 2D Accelerator
  - Built-in hardware command queue, Direct Draw Accelerato and GDI 2000 Accelerator

- Supports burst frame buffer read/write for SDRAM / SGRAM
- Supports auto SGRAM block write Bitblt function for engine acceleration
- Built-in 64x64x16 bit-mapped blended color hardware cursor

- Maximum 32MB frame buffer with linear addressing
- Built-in engine write-buffer with byte-merge
- Built-in source read-buffer to minimize engine wait-state
- Display Memory Interface
- Supports SDR SDRAM, DDR SDRAM, SDR SGRAM and DDR SGRAM
- Supports 8 MB, 16 MB, 32 MB memory configurations
- Supports 2Mx32, 1Mx16, and 4Mx16 SDRAM types up to 143 MHz with 1.14 GB/s bandwidth
- Supports 1Mx32, 2Mx32 SGRAM types up to 143 MHz with 1.14 GB/s bandwidth
- Supports 4Mx16, DDR SDRAM or 1Mx32, 2Mx32 DDR-SGRAM types up to 143 MHz with 2.28 GB/s bandwidth
- Support bi-directional data strobe type DDR SDRAM and DDR SGRAM
- Supports internal 256-bit display memory path, DRAM auto memory size/type detecting, ping-pong banking operation by 8 bank registers, SGRAM block write operation, asymmetric DRAM size configurations and tile-base DRAM address mapping.